WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory array including a plurality of memory cells arranged in a matrix;

a refresh timer circuit providing a refresh request signal at a time interval required to refresh data held by said plurality of memory cells;

a command generation circuit generating an internal command signal according to an access command; and

a row selection control circuit carrying out an operation associated with row selection of said memory array according to said internal command signal and said refresh request signal, said row selection control circuit including

a timing control circuit rendered active according to said internal command signal to output timing signals of a row selection operation of said memory array,

a refresh control circuit receiving and holding said refresh request signal to output an internal refresh command signal when said timing control circuit attains an inactive state, and

a refresh timing control circuit rendered active according to said internal refresh command signal to output said timing signal instead of said timing control circuit; and

a row selection circuit carrying out row selection of said memory array according to said timing signal.

2. The semiconductor memory device according to claim 1, wherein said access command includes a read command,

wherein a basic cycle time of said semiconductor memory device starting from reception of said access command up to attaining a state that allows reception of the next access command is at least a total time of a normal read cycle time starting from output of said internal command signal up to completion of data read out from said memory array and a refresh cycle time starting from output of said internal refresh command signal up to

completion of refresh of a portion in said memory array corresponding to said internal refresh command signal.

3. The semiconductor memory device according to claim 2, wherein said refresh control circuit comprises

a latch circuit receiving and holding said refresh request signal, and

a pulse generation circuit providing a pulse that becomes a basis of said internal command signal when an output of said latch circuit indicates input of said refresh request signal and said timing control circuit is at an inactive state.

4. The semiconductor memory device according to claim 2, wherein said command generation circuit holds said access command, and waits for inactivation of said refresh timing control circuit to output said internal command signal when said refresh timing control circuit is active.

5. The semiconductor memory device according to claim 4, wherein said command generation circuit comprises

a latch circuit receiving and holding said access command, and

a pulse generation circuit providing a pulse that becomes a basis of said internal command signal when an output of said latch circuit indicates input of said access command and when said refresh timing control circuit is at an inactive state.

6. The semiconductor memory device according to claim 2, wherein said command generation circuit comprises

an internal command generation circuit providing a command generation reference signal according to said access command, and

a delay circuit delaying said command generation reference signal for at least said refresh cycle time and providing said internal command signal,

wherein said refresh control circuit receives and holds said refresh request signal to output said internal refresh command signal when said

timing control circuit attains an inactive state.

7. The semiconductor memory device according to claim 6, wherein said refresh control circuit comprises

a latch circuit holding said refresh request signal, and

a pulse generation circuit providing a pulse that becomes a basis of said internal refresh command signal when an output of said latch circuit indicates input of said refresh request signal and when said timing control circuit attains an inactive state.

8. The semiconductor memory device according to 2, further comprising a data input/output control circuit receiving and holding as read out data an output from said memory array, and receiving an output enable signal to output said read out data.

9. The semiconductor memory device according to claim 2, wherein said row selection control circuit further comprises

an address latch circuit holding an applied row address to output a normal row address,

a refresh counter circuit sequentially updating and providing a refresh row address corresponding to a row to be refreshed, and

a select circuit receiving said normal row address and said refresh row address to output one of said normal row address and said refresh row address as an address corresponding to row selection of said memory array according to said internal refresh command signal.

10. The semiconductor memory device according to claim 9, wherein said memory array includes a plurality of banks that allows a row select operation independently,

wherein said refresh control circuit outputs said internal refresh command signal after said refresh control circuit attains an inactive state when a bank indicated by said normal row address coincides with a bank indicated by said refresh row address.

11. The semiconductor memory device according to claim 9, wherein said address latch circuit accepts said applied row address in synchronization with a clock signal.

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12. The semiconductor memory device according to claim 2, further comprising a latch circuit accepting said access command in synchronization with a clock signal and providing said access command to said command generation circuit.

13. A semiconductor memory device comprising:

a memory array including a plurality of memory cells arranged in a matrix;

a command detection circuit providing a command detection signal indicating that an access command has been applied to said memory array and an internal command signal corresponding to said access command; and

a row selection control circuit carrying out an operation related to row selection of said memory array according to said internal command signal,

said row selection control circuit including

a retain circuit accepting an applied row address according to said command detection signal to retain the applied row address as an internal row address, and

a comparison circuit comparing said row address with said internal row address at an elapse of a first predetermined time upon detection of change in said row address to determine whether said internal row address is to be used in row selection of said memory array.

14. The semiconductor memory device according to claim 13, wherein said comparison circuit comprises

an address change detection circuit detecting a change in said row address,

a delay circuit delaying an output of said address change detection circuit for said first predetermined time, and

an address comparison unit comparing said row address with said internal row address according to an output of said delay circuit.

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15. The semiconductor memory device according to claim 14, wherein said address comparison unit designates said retain circuit to accept again said row address when a result of address comparison corresponds to mismatch.

16. The semiconductor memory device according to claim 13, wherein said comparison circuit designates said retain circuit to accept again said row address when said row address does not match said internal row address,

wherein said row selection control circuit further includes a delay circuit inhibiting update of said internal row address to said retain circuit at an elapse of a second predetermined time in response to said command detection signal.

17. The semiconductor memory device according to claim 16, wherein said second predetermined time is half a basic cycle time which is a period of time starting from said semiconductor memory device receiving said access command up to receiving the next access command.